Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 52438

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2017

Third Semester

Electronics and Communication Engineering

EC2203 – DIGITAL ELECTRONICS

(Regulations 2008)

(Common to PTEC 2203 – Digital Electronics for B.E. (Part-Time) Third Semester – ECE – Regulations 2009)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A (10×2=20 Marks)

1. Name the two canonical forms of Boolean algebra.
2. Why digital circuit are more frequently constructed using NAND or NOR gates than with AND and OR gates ?
3. What is the difference between half adder and full adder ?
4. What do you mean by a magnitude comparator ?
5. Define race around condition.
6. Define shift registers.
7. State the types of ROM.
8. What is programmable logic array ? How it differs from ROM ?
9. Give the comparison between synchronous and asynchronous sequential circuit.
10. What is fundamental mode sequential circuit ?

PART – B (5×16=80 Marks)

11. a) Obtain the minimum SOP using quine Mc Clusky's method and verify using K map. $F = m_0 + m_2 + m_4 + m_8 + m_9 + m_{10} + m_{11} + m_{12} + m_{13}$. (16)

(OR)

b) A majority gate is a digital circuit whose output is equal to 1, if the majority of inputs are 1's. The output is '0' otherwise using a truth table find the Boolean function implemented by a 3-input majority gate. Simplify the function and implement with gates. (16)

12. a) Design and implement a full adder circuit and a full subtractor circuit. (16)

(OR)

b) i) Implement a full adder circuit using decoder and using multiplexer. (8)

ii) Design a 2 bit magnitude comparator. (8)

13. a) Design a mod 6 counter using FFS. Draw the state transition diagram of the same. (16)

(OR)

b) A sequential circuit with 2D FF's A and B and input X and output Y is specified by the following next state and output equations.

$A(t + 1) = AX + BX$

$B(t + 1) = A'X$

$Y = (A + B) X'$

i) Draw the logic diagram of the circuit, (5)

ii) Derive the state table, (5)

iii) Derive the state diagram. (6)

14. a) Discuss on the concept of working and applications of the following memories

i) ROM (10)

ii) EPROM. (6)

(OR)

b) Describe the operation and application of

i) PLD (8)

ii) FPGA. (8)

15. a) A sequential circuit has four FF's ABCD and an input x is described by the following state equations.

$A(t+1) = (C\overline{D} + \overline{C}D)x + (CD + \overline{CD})x$

$B(t+1) = A$

$C(t+1) = B$

$D(t+1) = C$

i) Obtain the sequence of states when x = 1 starting from state ABCD = 0001 **(8)**

ii) Obtain the sequence of states when x = 0 starting from state ABCD = 0000. **(8)**

(OR)

b) Develop the state diagram and primitive row flow table for a logic system that has two inputs S and R and a single output 'Q'. The device is to be an edge triggered SR flip flop but without a clock. The device changes state on the rising edges of the two inputs. Static input values are not to have any effect in changing the Q output. **(16)**